G-COE PICE, International Symposium and
IEEE EDS Minicolloquium on
Advanced Hybrid Nano Devices (IS-AHND) 2011

CMOS-Device Technology Benchmarks for Low-Power Logic LSIs

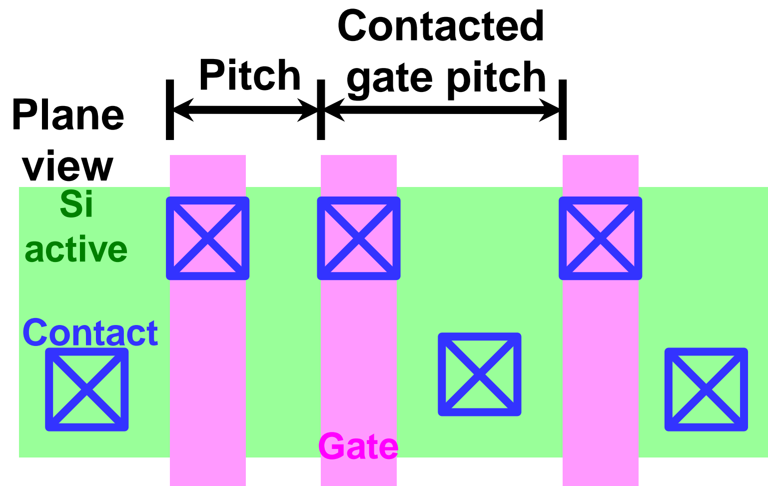
Oct./4th, 2011 (35 min.)

Hitoshi Wakabayashi, Sony Corporation

- Benchmarks of CMOS scaling
  - Cost ← chip size
  - Power
  - Speed

ITRS Logic Roadmap

- **International Technology Roadmap for Semiconductors** http://www.itrs.net/
- **Half-pitch scaling**
  - ◆**Cost, Power, Speed**



x 0.7 x 0.7

180 ➔ 130➔ 90 ➔65 ➔ 45(40)

X 0.5 N-1 N N+1

➔ 32(28) ➔ 22(20) ➔ 16(14)

➔ 11-nm technology node

- 2011 SSDM

Feature size [nm]

200
100
80
60
40
20
10
9
7

2000 2005 2010 2015 2020 2025

Years

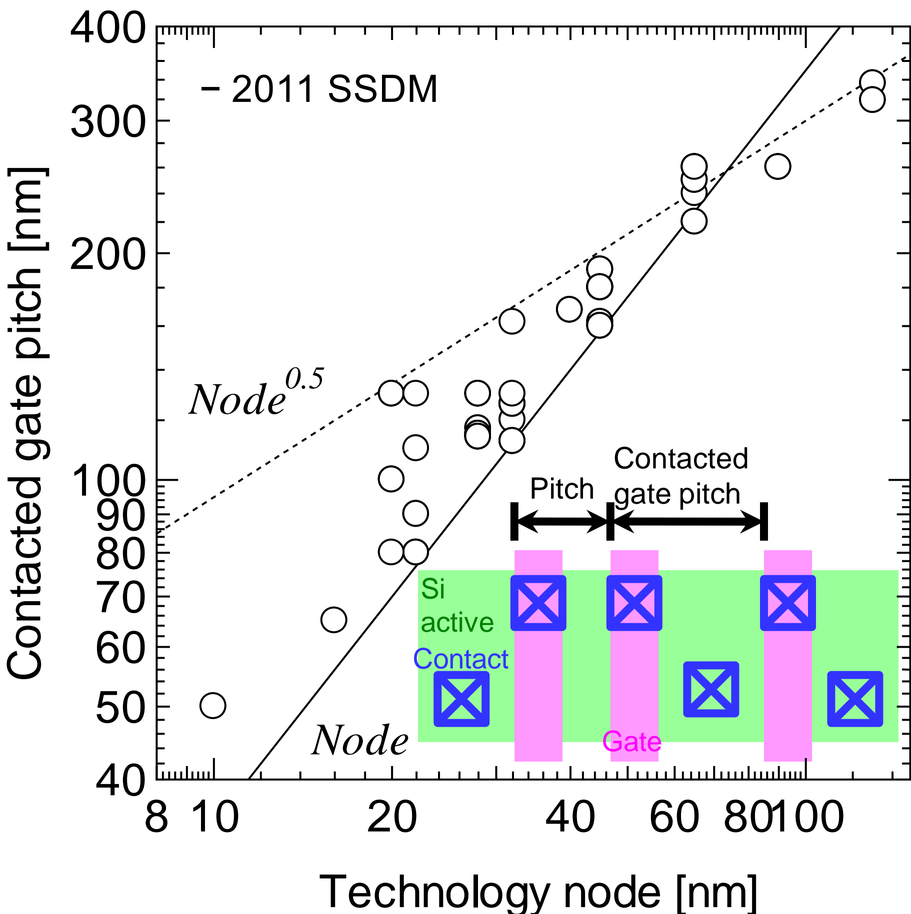
Half pitch production year ITRS 1999−2009 x0.7/3−years

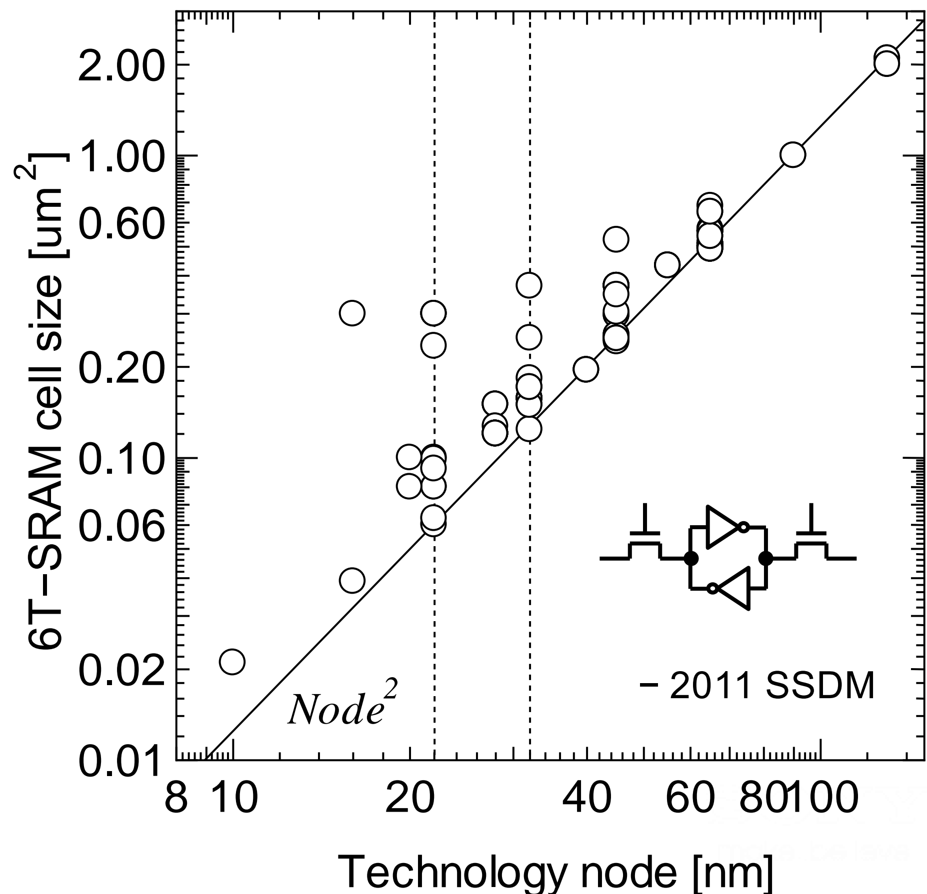
Tech. node publish years

Tech. node Intel products x0.7/2−years

cost reduction by scaling

■ Pitch scaling ➔ SRAM-cell-size scaling



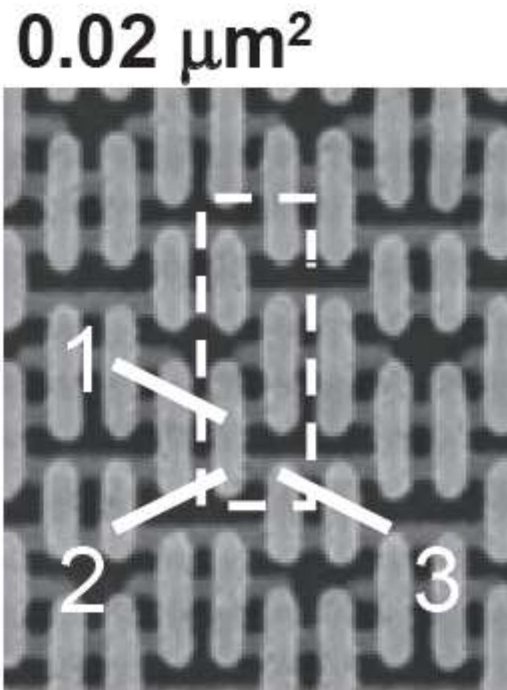


10 nm, 0.021 um2, IBM, 11VL T4-5

- The world smallest 6T-SRAM
- FinFET u/ Mixed EB and Optical litho. (MXL)
- Contacted gate pitch (CGP) scaling down to 50 nm

CGP (nm)	CFP (nm)	x (µm)	y (µm)	area µm²	β
50	50	0.21	0.10	0.021	1
60	50	0.21	0.12	0.025	1
70	50	0.21	0.14	0.029	1
70	50/60	0.25	0.14	0.035	1

Fig 2: Design rules for the 6T SRAM bitcells investigated in this work. Varying combinations of contacted gate pitch (CGP) and contacted fin pitch (CFP) from 70 to 50 nm were used to explore the behavior of bitcells with areas ranging from 0.035 to 0.021 μm^2 with β ratios of 1.



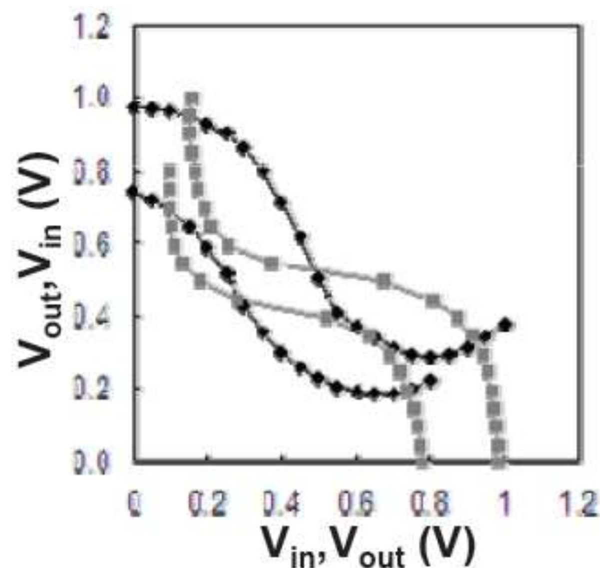
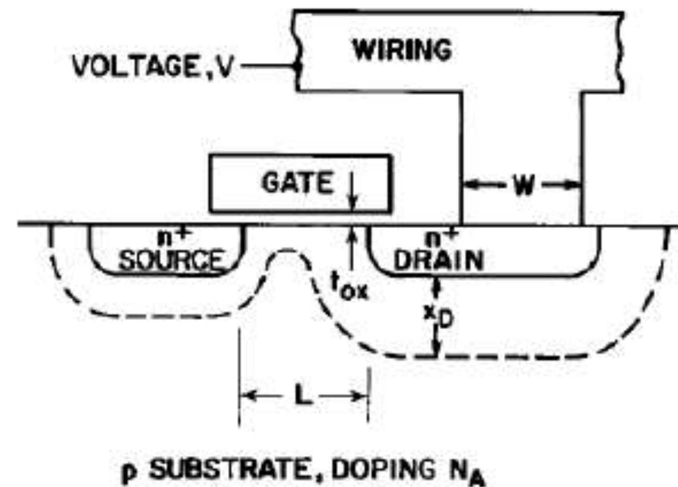


Fig 15: Demonstration of a 0.021 μm^2 bitcell with a CGP and CFP of 50 nm

Performance comparison

- **Delay time**
  - ◆ (Cg+Cpara) Vdd / Ids = Cpara x Vdd / Ion @ Cg << Cpara
    = Ci x Lg x Vdd / Ion @ Cg >> Cpara
  - ◆ Ieff
- **Power density [W/um2]**
  - ◆ Active $fCV^2 = I/CV \times CV^2$ = Vdd x Ion [A/um] / Lg [um]
  - ◆ Standby J_leak x Vdd

Device or Circuit Parameter	Scaling Factor
Device dimension *tox, L, W*	$1/\kappa$
Doping concentration *Na*	κ
Voltage *V*	$1/\kappa$
Current *I*	$1/\kappa$
Capacitance $\varepsilon A/t$	$1/\kappa$
Delay time/circuit *VC/I*	$1/\kappa$
Power dissipation/circuit *VI*	$1/\kappa^2$
Power density *VI/A*	1

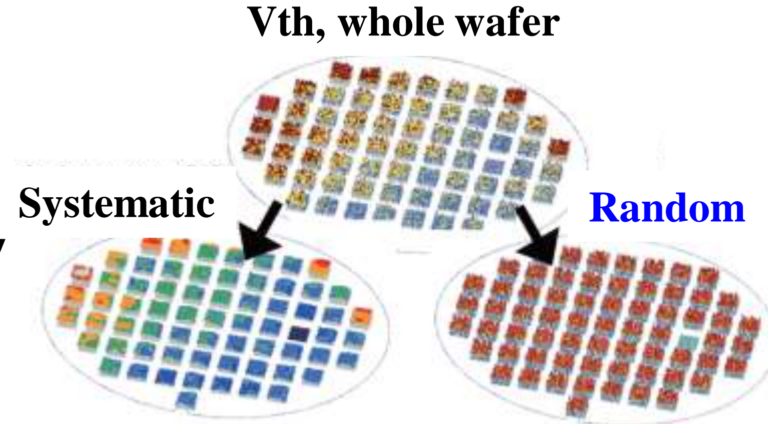


R. Dennard, IEEE JSSC, 1974

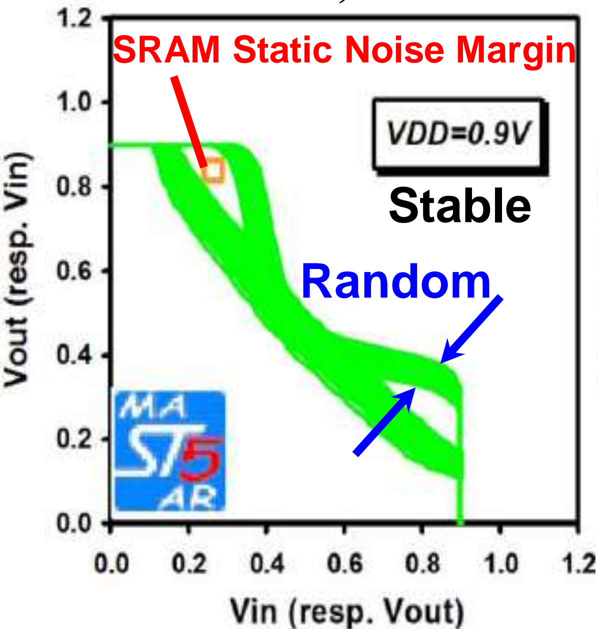
Voltage-scaling limited by random variability

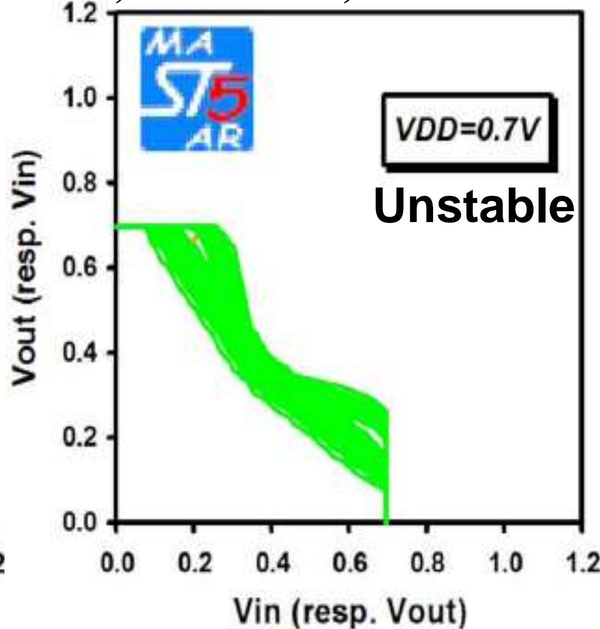
- Threshold voltage (Vth) variability
  ➔ SRAM variability
  - ◆Systematic 🡐 un-uniformity
  - ◆Random 🡐 Quantization

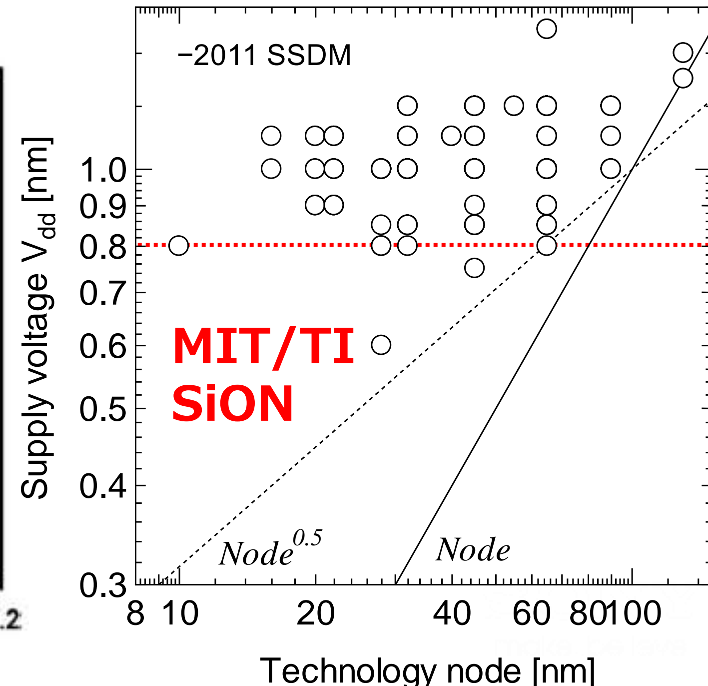
M. Kanno, Sony, 2007 VLSI Tech.



T. Skotnicki, STMicroelectronics, IEEE T-ED, 2008.

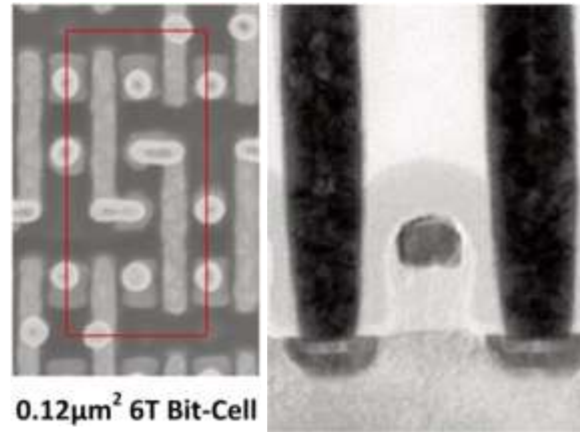




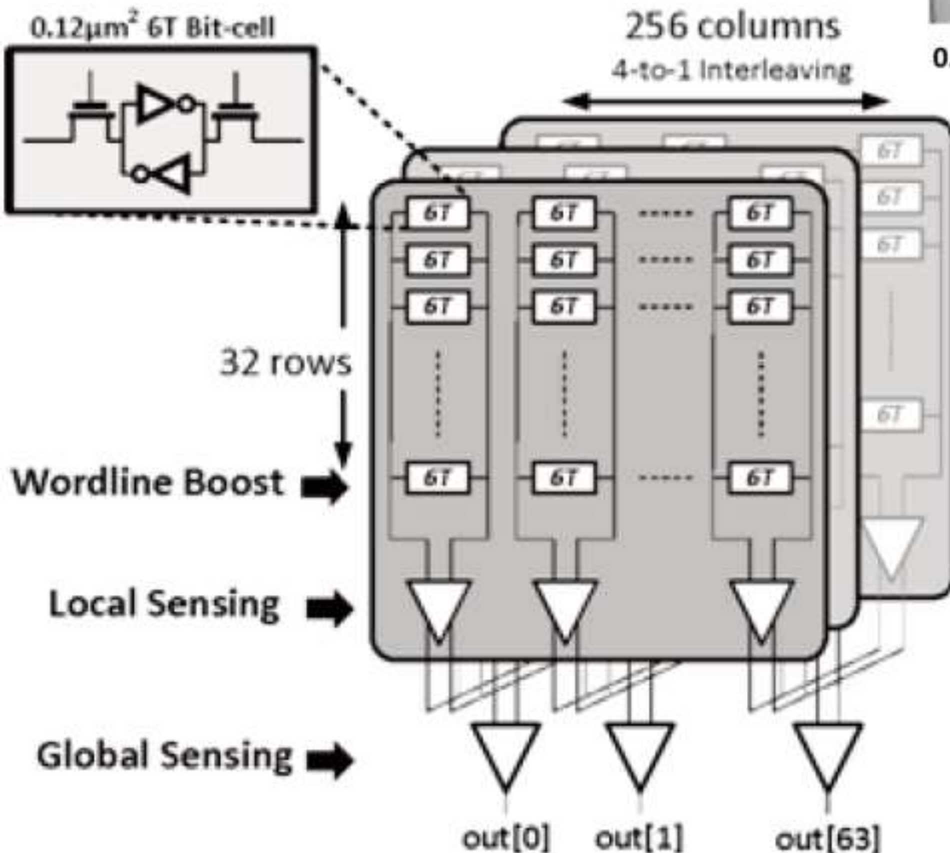


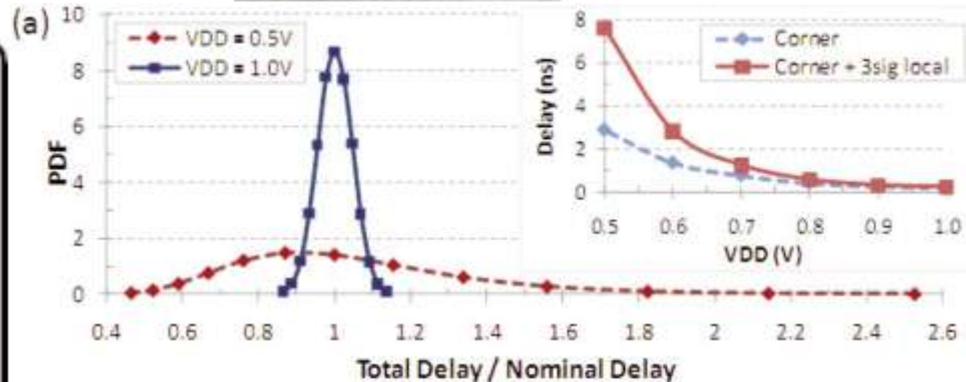
28nm, 0.6 V SoC, MIT/TI, ISSCC11 7.5/14.4

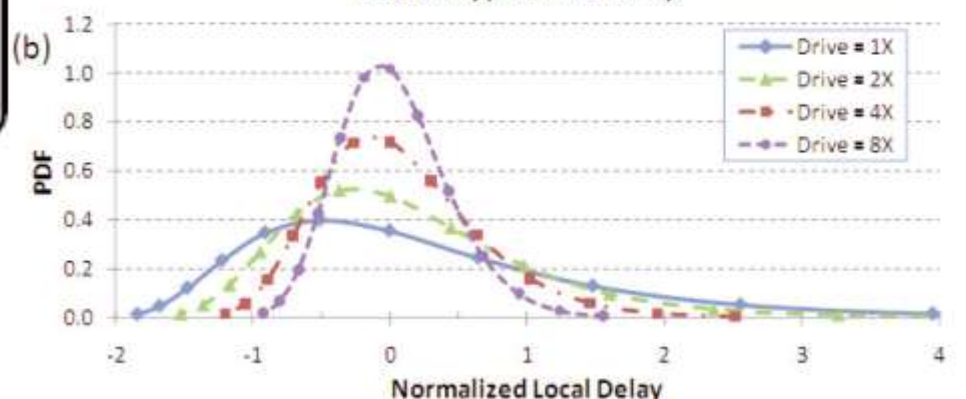
- Poly-Si/SiON, 6T-SRAM
- 3σ, 0.6V



Process	28nm Low Power CMOS
Lithography	high-NA 193i
Performance	pMOS: Epitaxial S/D SiGe
	nMOS: Strain techniques
Gate stack	dual-gate poly/SiON
	double patterning
Metal stack	ULK dual damascene
	Thick top Cu level and Al level
Logic	SVT, LVT, multi-channel length
Bit	0.12µm² 6-T SRAM bitcell





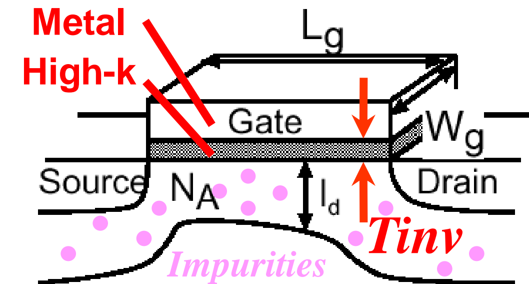


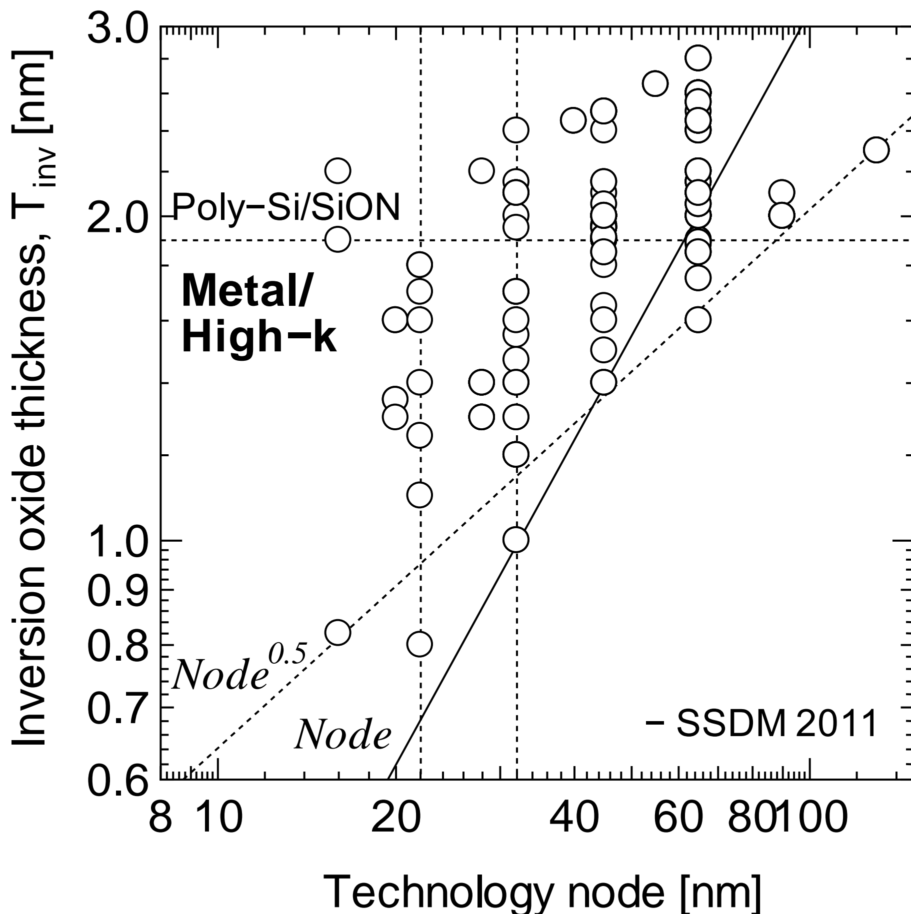
To reduce random variability

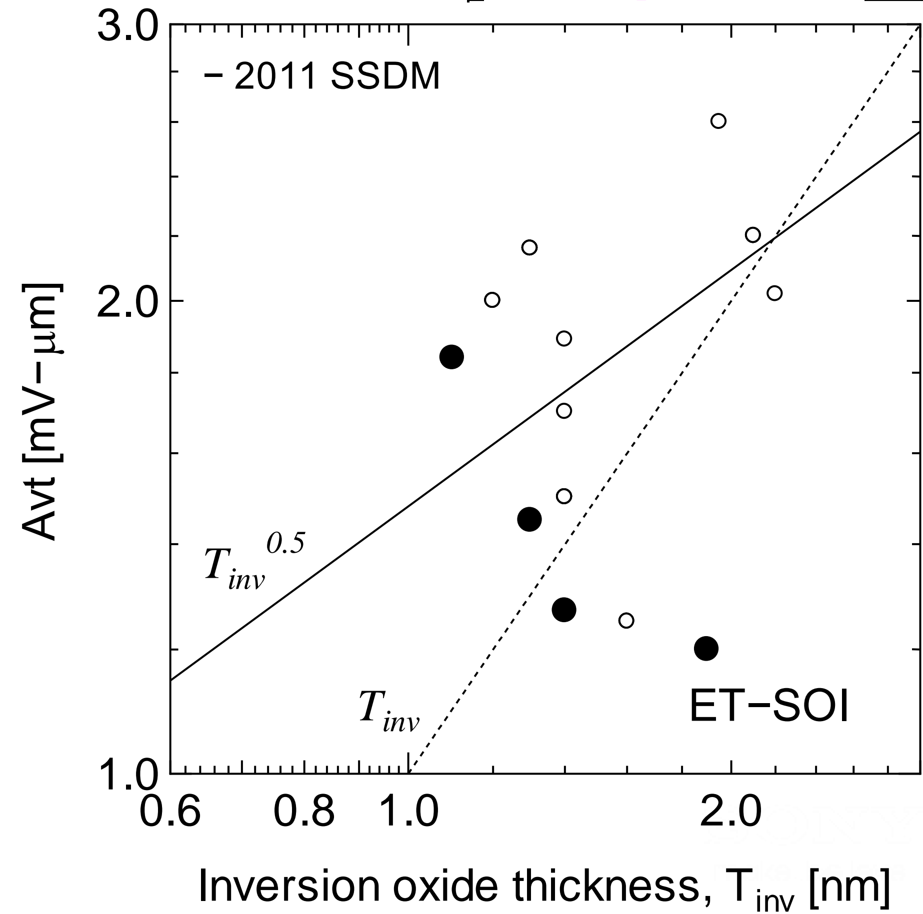
- **Sigma of threshold voltage**

  $\sigma Vth \propto \{Tinv\ Na^{1/4}\} / sqrt(Lg \times W) = Avt / sqrt(Lg \times W)$

- ***Metal/High-k gate stack***







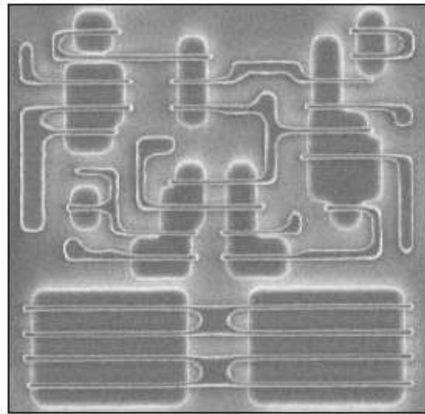
Variability reduction, Intel gate-last

- Thin Tinv by M/Hk gate
- Gridded layout

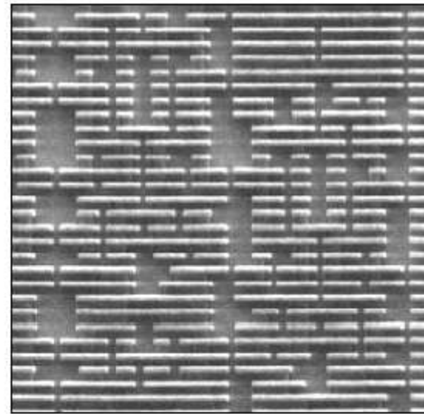
Layout Restrictions

M. Bohr, Intel, ISSCC, 2009

65 nm Layout Style



32 nm Layout Style

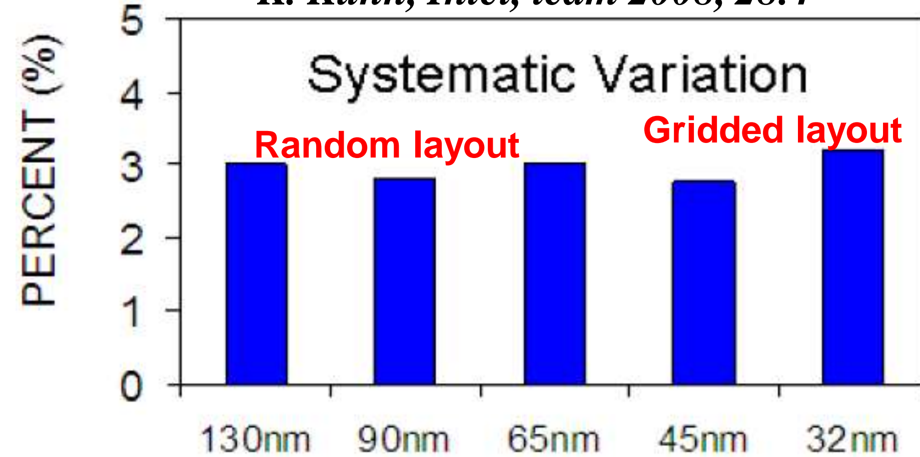


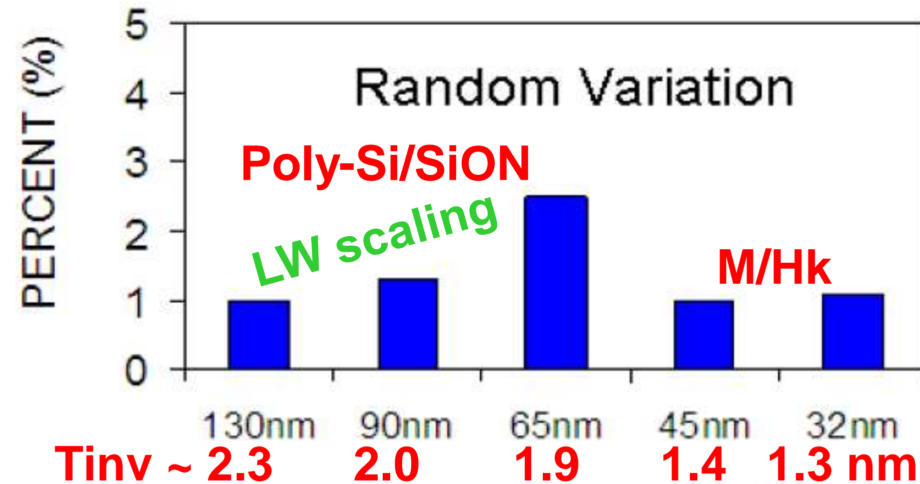
After gate pattering

- Bi-directional features
- Varied gate dimensions
- Varied pitches

- Uni-directional features
- Uniform gate dimension
- Gridded layout

K. Kuhn, Intel, iedm 2008, 28.4

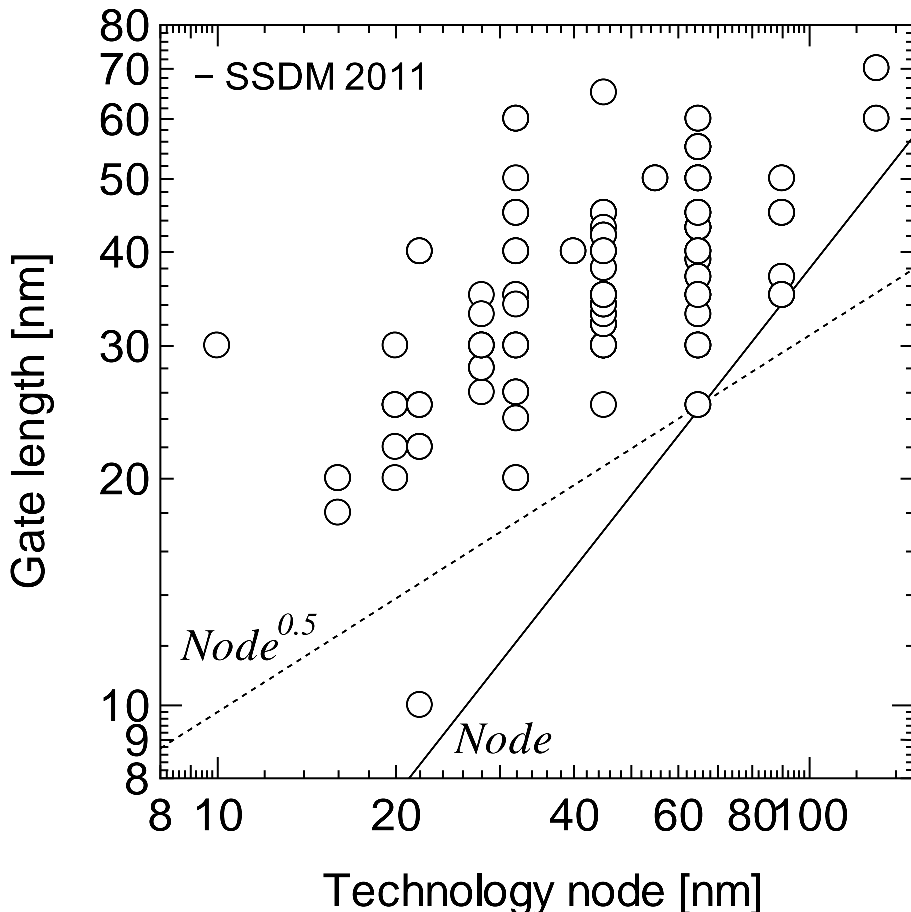




Tinv ~ 2.3 2.0 1.9 1.4 1.3 nm

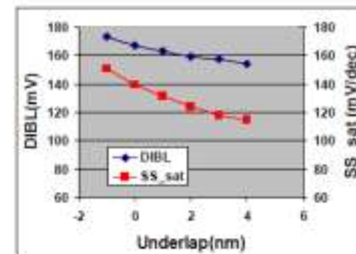
Gate capacitance reduction by Lg scaling

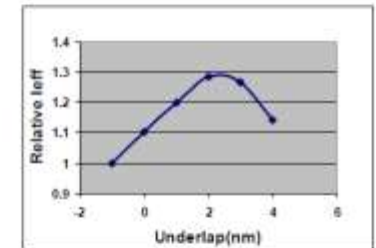
- *CV/I [sec] = Ci [F/um2] x Lg [um] x Vdd / Idsat [A/um]*
- **Lg scaling by thin Tinv u/ M/Hk gates**



M. Khare, IBM, iedm 2010, Short Course

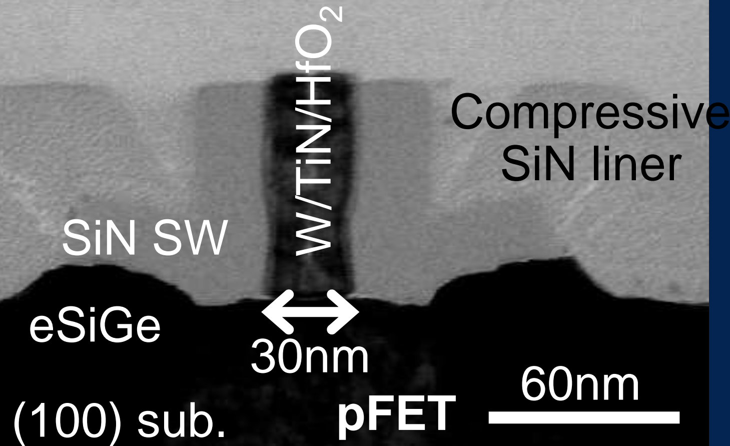
Electrostatics and Under-lap device in 15nm

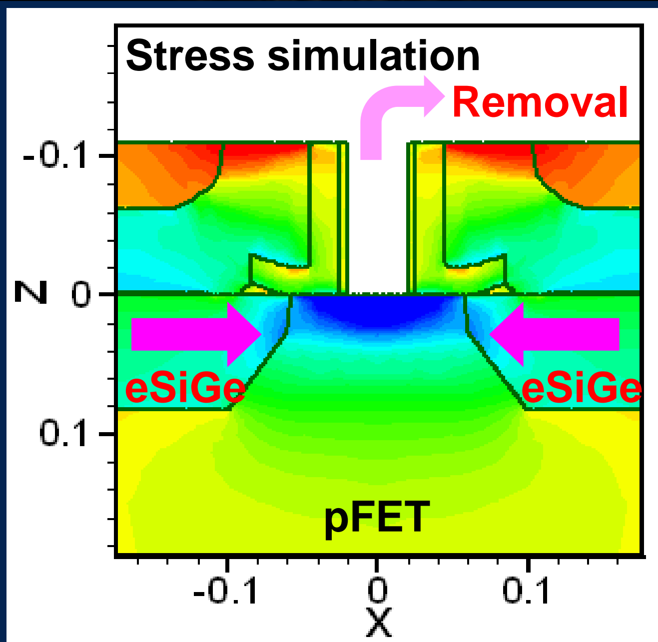


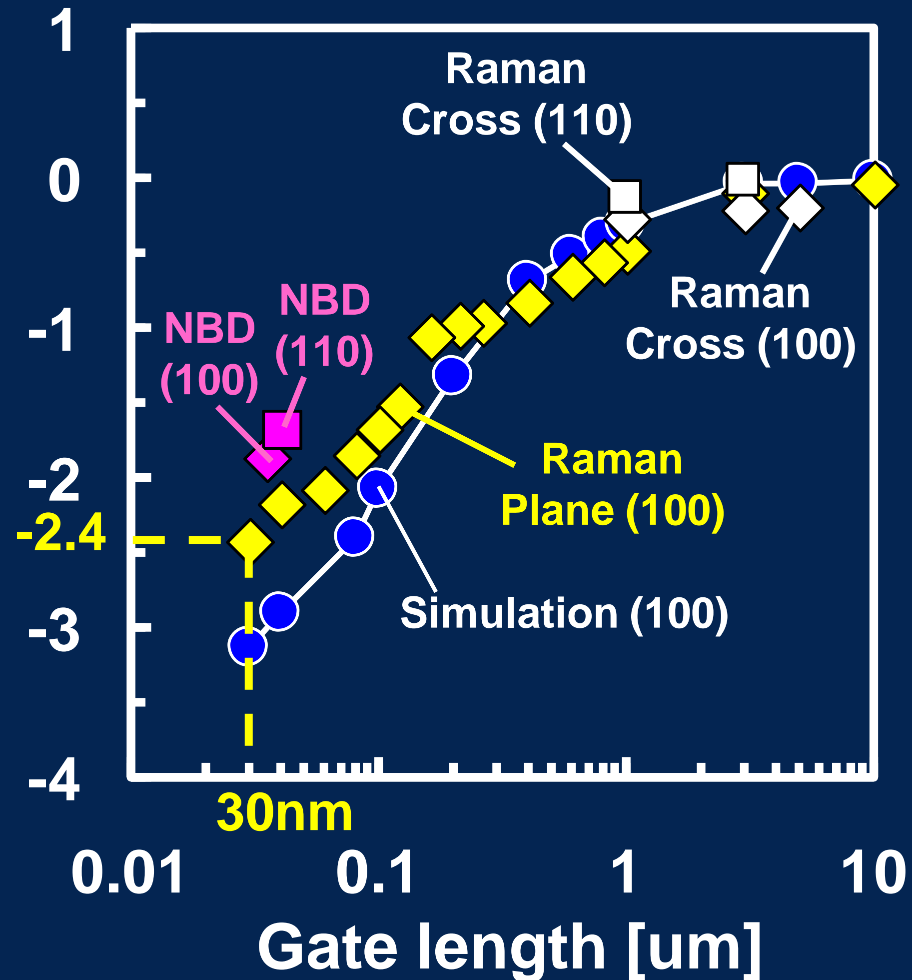


- Effect of under-lap junction on 15nm device electrostatics
  - SS shows improvement with under-lap condition
  - DIBL shows less impact as doping decreases as L increases
- Ieff vs under-lap plot shows Electrostatics vs External Resistance Trade-off
- Under-lap can help electrostatics if initial SCE is poor

Sony's Gate-Last M/Hk, VL09 T2A-1

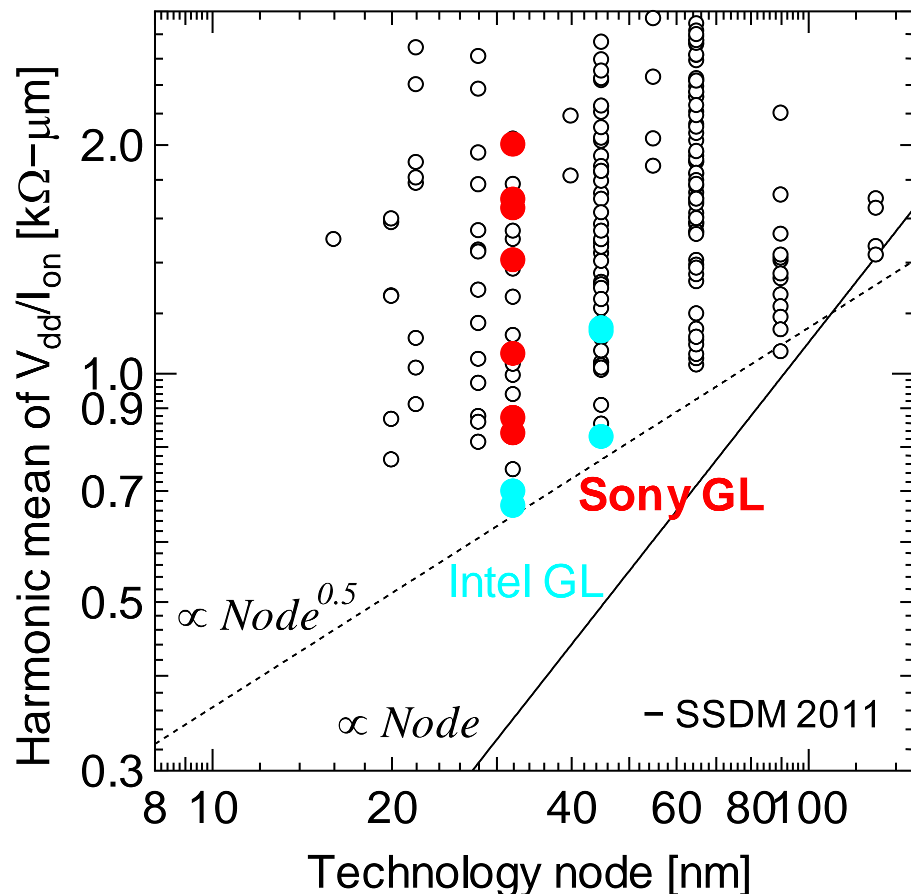


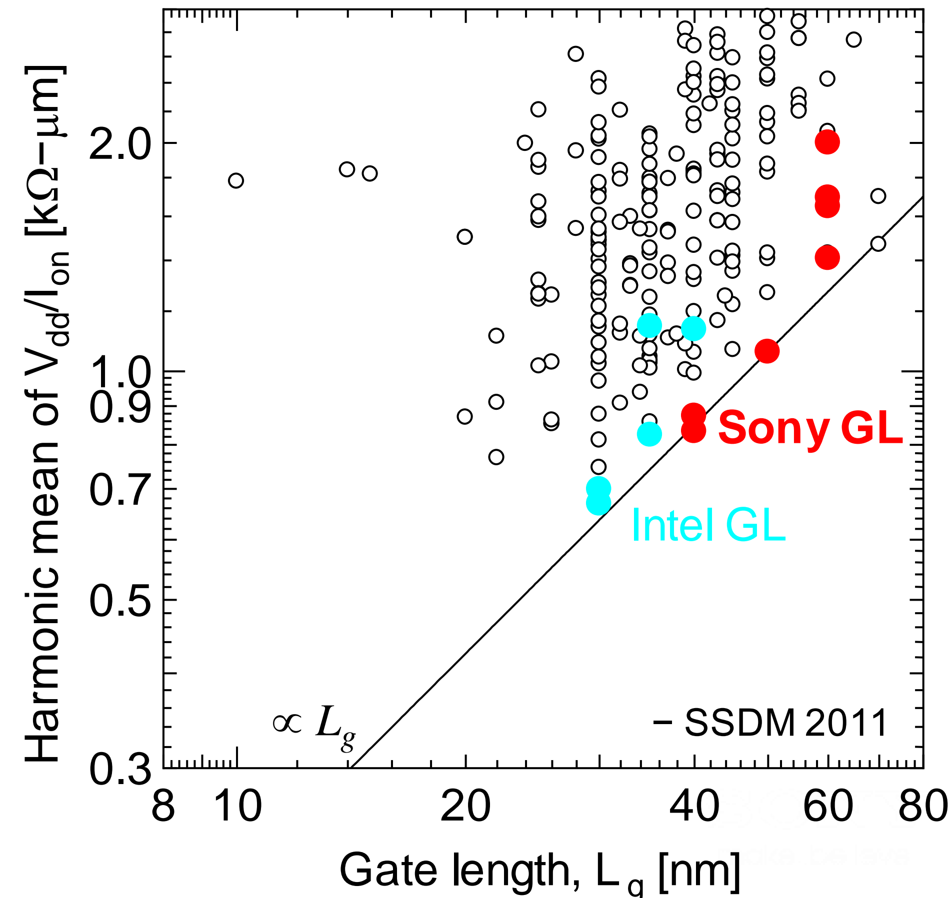




V/I vs. Node/Lg for HP/LOP/LSTP

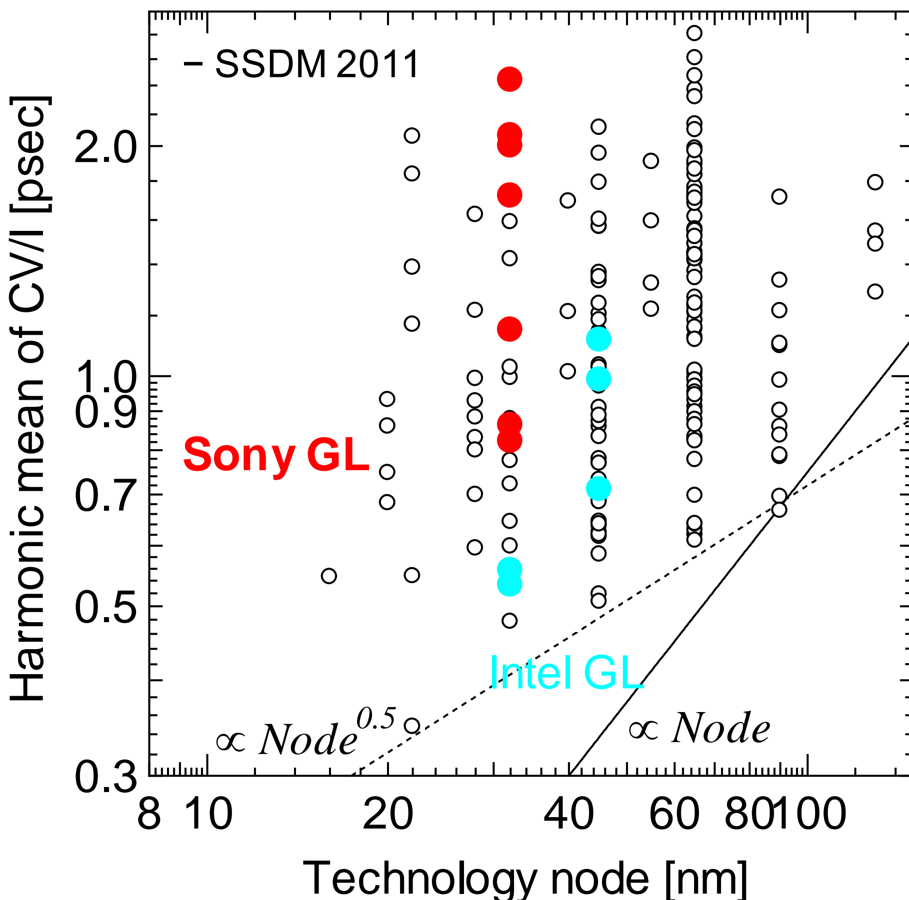
- **M/Hk gate-last achieves small V/I.**
- **FinFET has almost the same effects.**

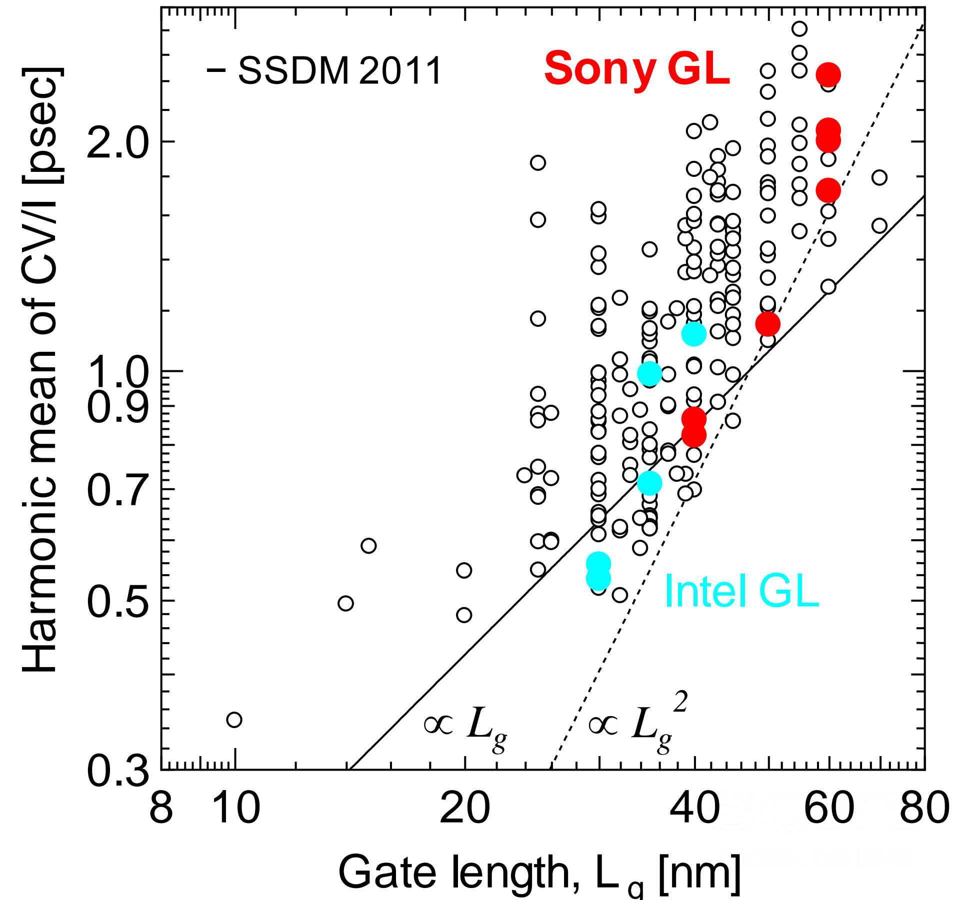




CV/I vs. Node/Lg

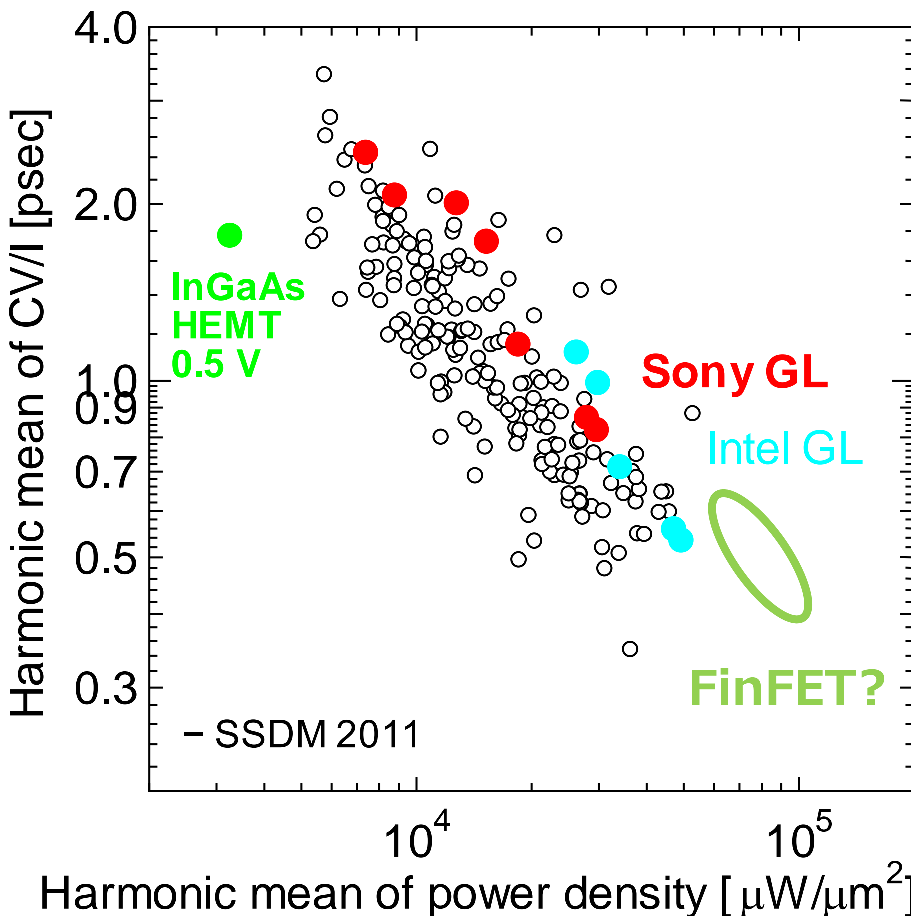
- **Slow down on node**
- **Speed up on Lg**
  - ◆ Slow Lg scaling
  - ◆ High-mobility pMOS

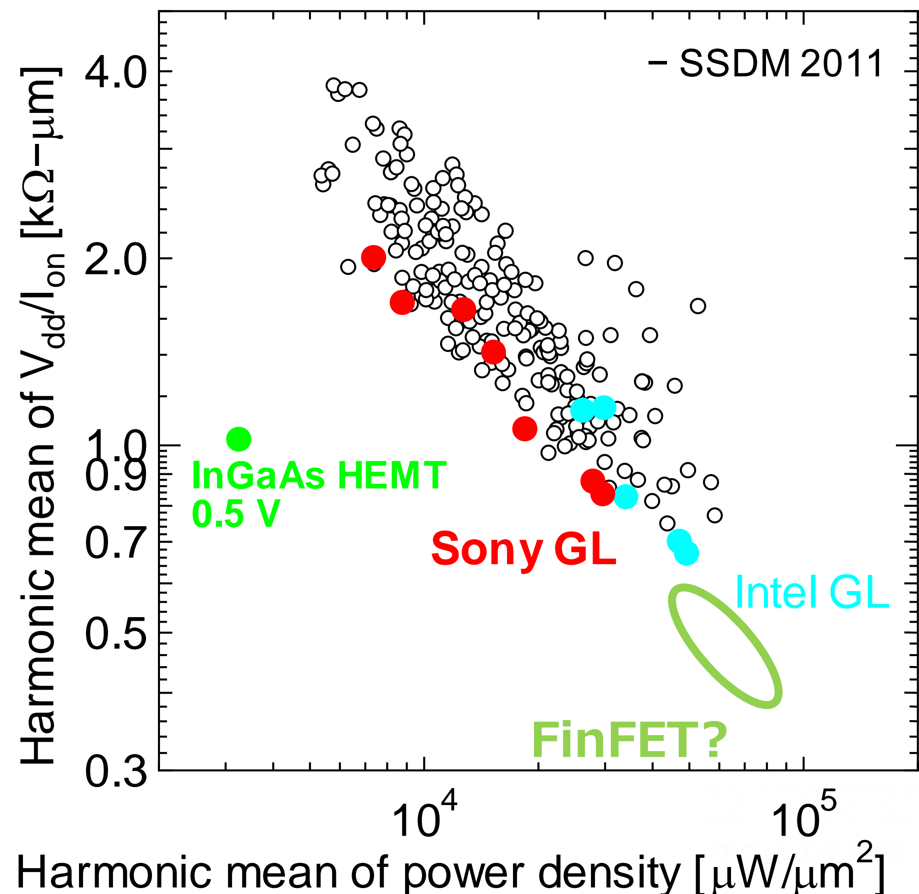




CV/I & V/I vs. power-density

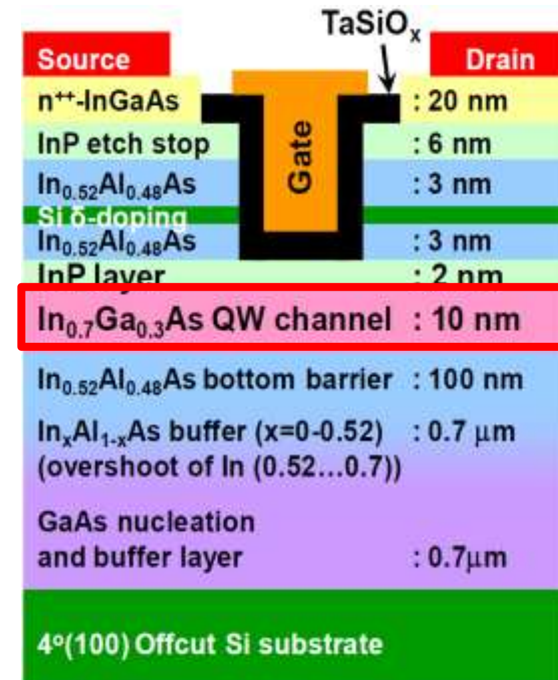
- Need low voltage based on high mobility



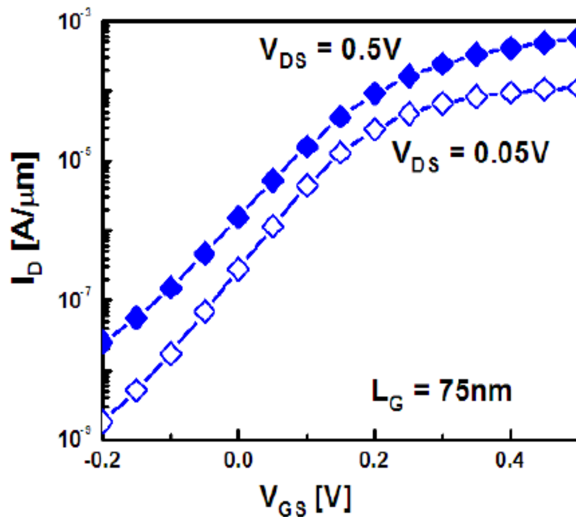


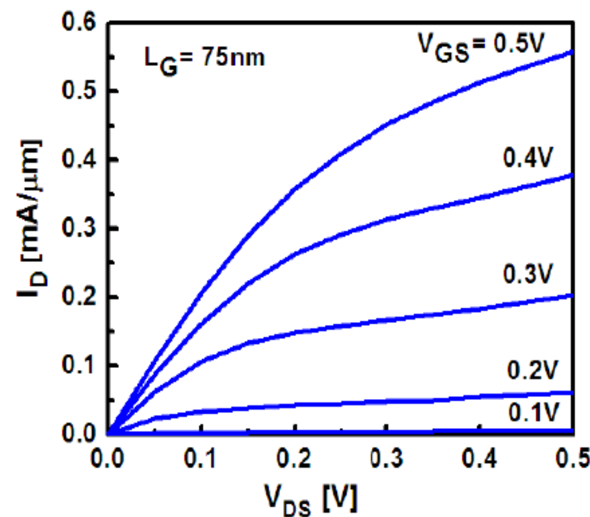
Voltage scaling by III-V, iedm09, 13.1

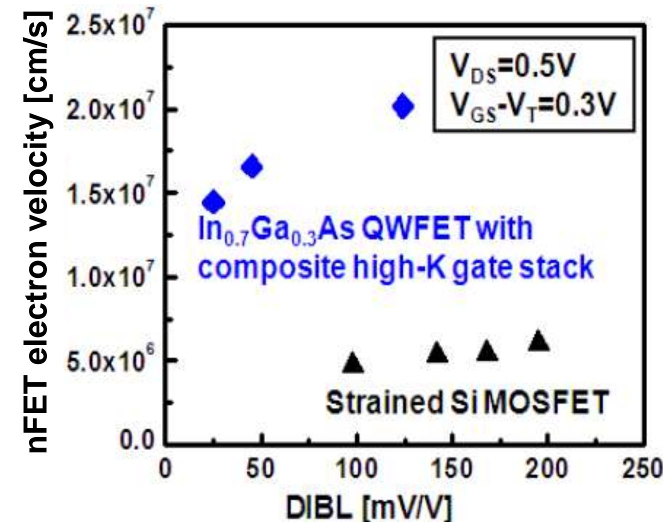
- **InGaAs HEMT on Si for nFET, Intel**
  - 10,000 cm2/Vs @ 300K
  - Lg = 75 nm
  - Vds = 0.5 V



iedm 09, 13.1, Intel

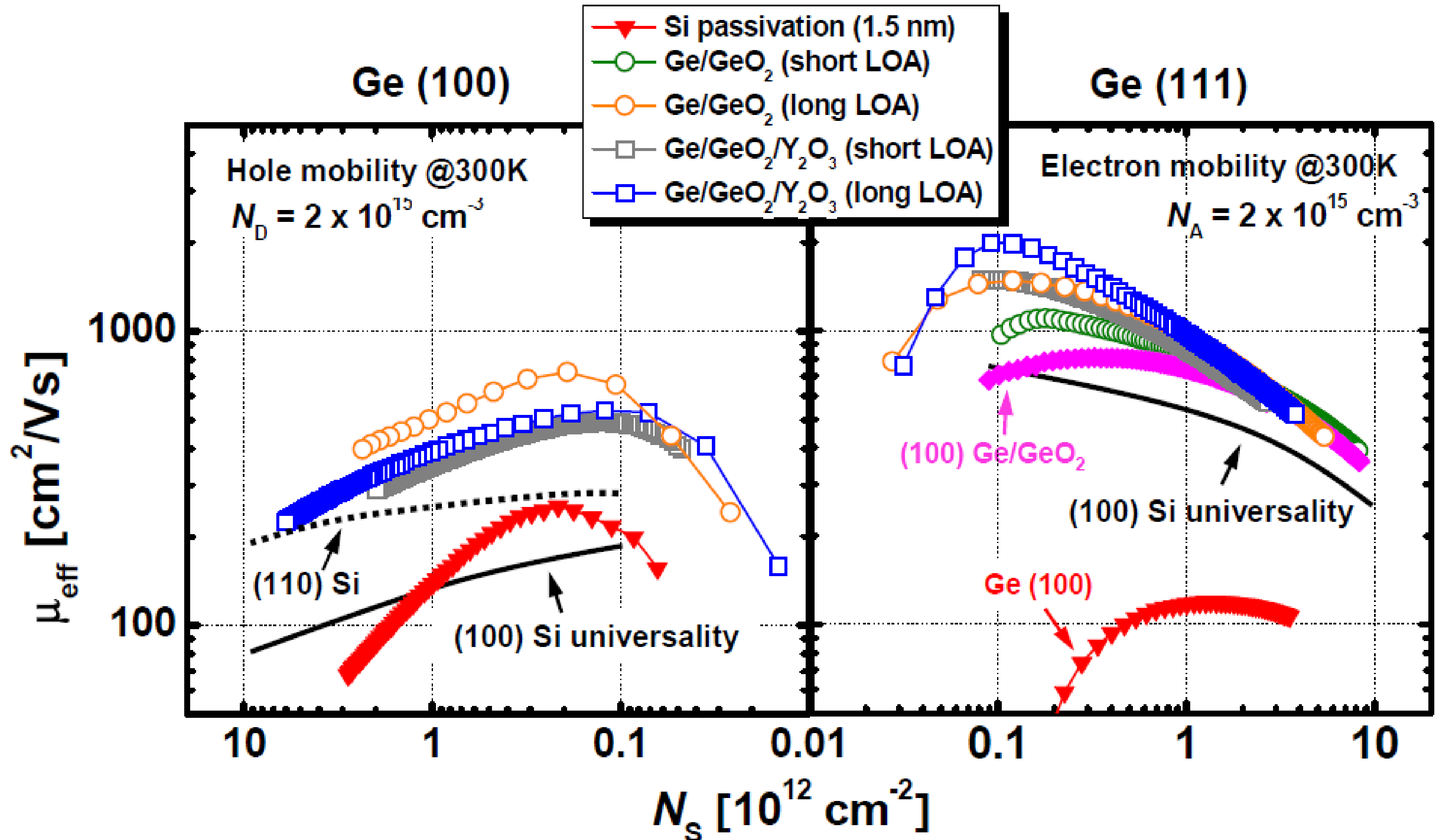






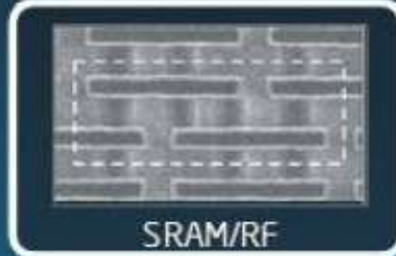
The highest μ Ge n/pFETs, iedm10 18.1

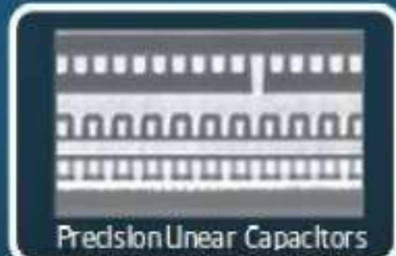
- Electron mobility: 1920 cm2/Vs
- Hole mobility: 725 cm2/Vs

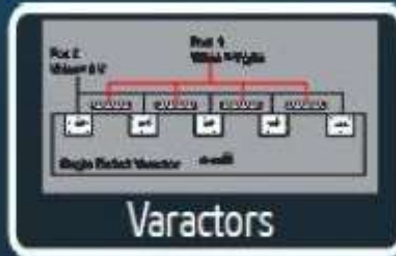


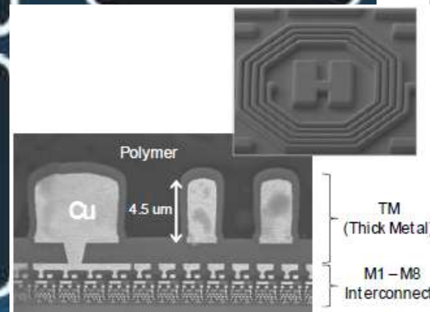
SoC components, Intel 45 nm

Intel web site









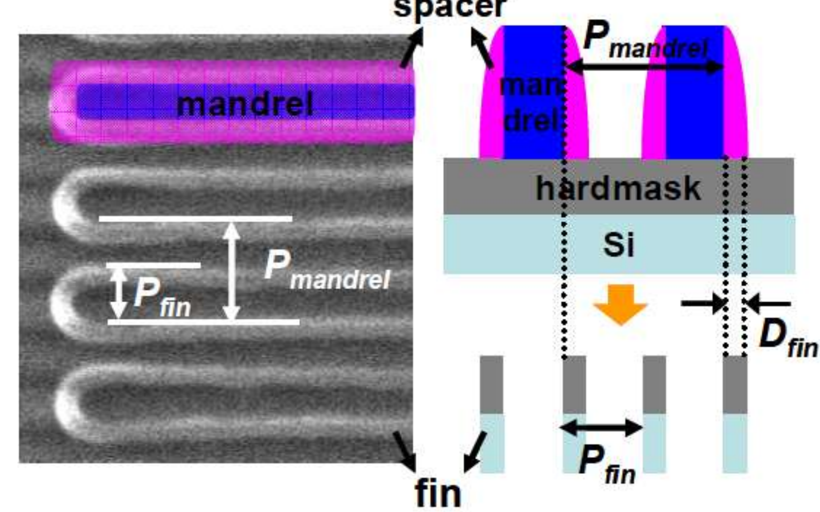
LOGIC TRANSISTOR	HIGH PERF
	STD PERF-PWR
	LOW PWR
	HIGH PERF/LOW PWR
I/O TRANSISTOR	1.8V
	2.5V
	3.3V
METALS	HIGH PERF (CPU)
	HIGH DENSITY
	LOW COST
	ULTRA HIGH DENSITY
EMBEDDED MEMORY	e-SRAM
	E-OTP/FUSE
BASIC ANALOG	MOM, MOS CAP
	INDUCTOR (L)
ADV MIXED SIGNAL/RF	PRECISION R
	PRECISION C
	HIGH Q L
	DEEP N W
	HIGH RES SUB

C.-H. Jan, Intel, iedm 2010, 27.2

Sidewall image transfer (SIT)

- Synchronized edges
  →Small variability

H. Kawasaki, iedm09, 12.1



. 5: The schematic of the SIT process. Fi

V. S. Basker, 2010 Symp. on VLSI Tech., 2.2

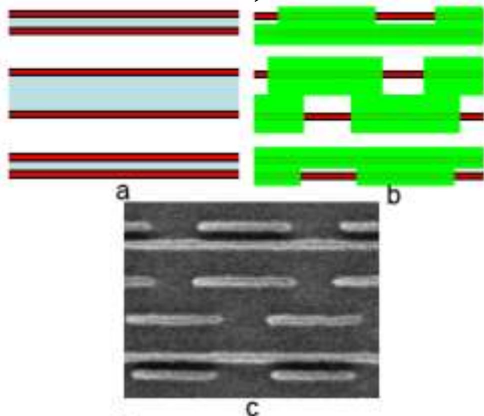
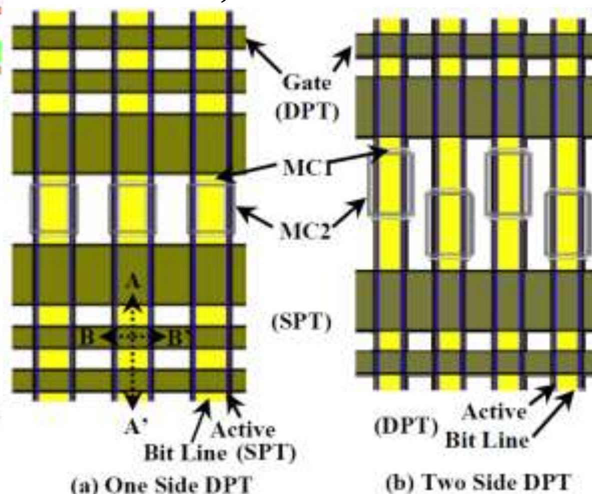
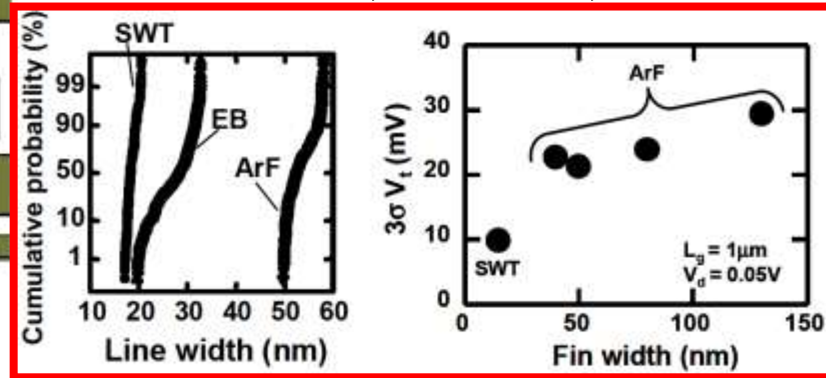


Fig. 3. DE[2] scheme for fin formation
(a) Fin formation by SIT process
(b) Cut process to get different fin pitch
(c) Top-down image of SRAM macro showing differential fin pitch.

Bong Tae Park, 2010 Symp. on VLSI Tech., 12.1



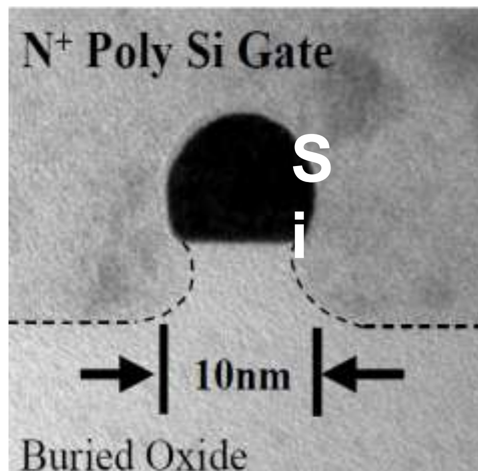
H. Kawasaki, IWJT 2007, S1-1



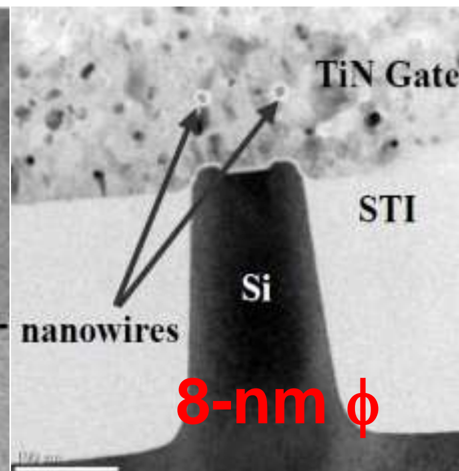
3D architectures

- **Requirements:**
  Idsat/Wfootprint > Idsat/Weff
  - ◆Single Si nanowire FET
  - ◆2D-twin Si nanowire FET
  - ◆3D stacked nanowire FET
- **Functionalities/chip area**
  - ◆SiP technologies

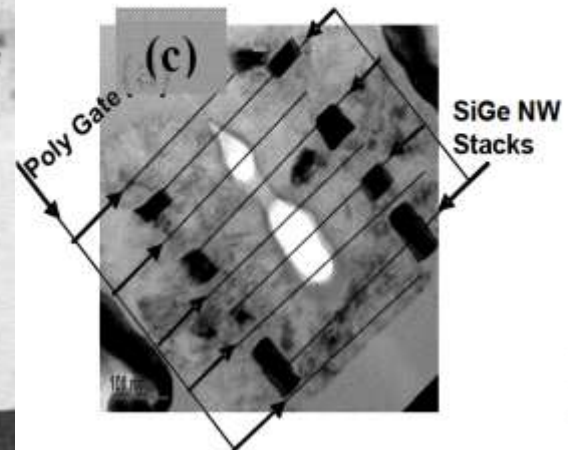
F.L. Yang et al., VLSI, 2004.



K.H. Yeo et al., IEDM, 2006.

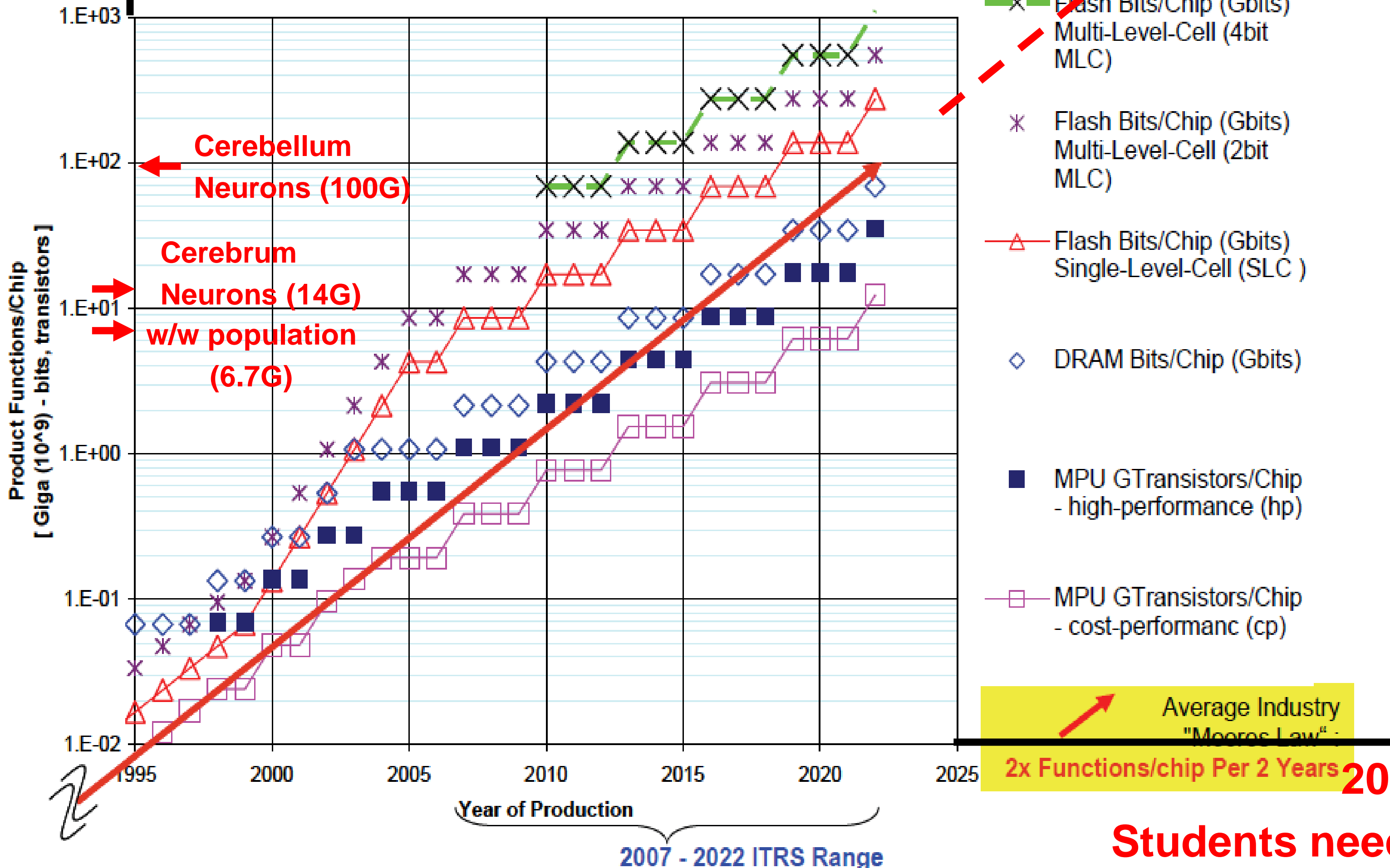


L.K. Bera, et al., IEDM, 2006.



Huge systems in a chip having 0.1-Peta Trs !!!

1E5 #/chip



Students need to consider.

Summary

- **Benchmarks of CMOS scaling**
  - **Cost**
  - **Power**
  - **Speed**